

In the Specification:

Please amend the paragraph beginning on page 1, line 17 as follows:

Current should flow ~~flows~~ through conductive structures with minimal resistance. However, due to geometry changes and material changes in the electrical path, higher resistances and higher current densities are experienced. These higher current densities can lead to detrimental mass transport between conductive interfaces at junctions between different conductive materials, as well as in the conductive materials themselves. Further, materials at the conductive interface may cause degradation of conductive characteristics at the interface due to mixing of atoms as a result of mass transport.

Please amend the paragraph beginning on page 10, line 17 as follows:

The probe is inserted through hole 28 and is connected to bond pad 20 over TV layer 16 and not over metal line 12. The offset of bond pad 20 also prevents direct damage to the metal line during wafer probe testing. Damage to metallization lines can affect current density and reliability of metal lines, and damage to a bond pad can result in difficulty connection a bond wire thereto or cause reliability problems later on. In accordance with the present invention, damage due to probing is no longer an issue since, the present invention provides an offset area or probe area 30 for probe contact which is separate for a bond area 32 (FIG. 2).

Please amend the paragraph beginning on page 11, line 11 as follows:

Referring to FIG. 3, to further illustrate the present invention probe area 30 and bond area 32 are shown. Bond area 32 is directly above interconnect 38 while probe area 30 is located over dielectric layer 16. When a probe contacts probe area 30, any damage derived therefrom does not

affect bond area 32 since a bonding wire is directly attached to bond area 32. Bond area 32 remains undamaged by probing which results in a better connection with a bonding wire (not shown) Further, barrier layer 18 is preserved since ~~[[and]]~~any force imparted to probe area 30 is applied over layer 16.

Please amend the paragraph beginning on page 11, line 21 as follows:

Referring to FIG. 4, a top view of a bond pad 20 is shown in accordance with the present invention. Bond pad 20 includes bond area 32 and probe area 30, which are separate as described above. Passivation layer 21 is patterned to expose bond area 32 and probe area 30. Passivation layer 21 is shown as a transparent layer so that underlying structures are visible. Passivation layer 21 includes layers 22, 24, and ~~possible~~possibly 25. Passivation layer 21 is patterned to create a border 19 between bond area 32 and probe area 30. Border 19 is preferably employed to prevent slipping of a probe onto the sensitive bond area 32. Border 19 may be formed ~~form~~from other materials as well for example, a raised portion of conductive material from the bond area or the probe area may be employed.

Please amend the paragraph beginning on page 13, line 9 as follows:

Referring to FIG. 5, a top view of an alternate embodiment is shown in accordance with the present invention. In this embodiment, probe area 30 and bond area 32 are continuous. This provides a larger available probing area. Probe area ~~[[32]]~~ 30 is employed for testing the semiconductor device while bond area ~~[[30]]~~ 32 is employed for attaching a bond wire to the semiconductor device for providing off-chip connections. It should be noted that probe areas and

bond areas are preferably formed as close as possible to interconnect 38 and metal line 12 to reduce electrical resistance for probe testing and ultimately for bond wire connections.